CLAIMS

We claim:

1. A method, comprising:

splitting a cache operation into two or more phases and two or more clock domains.

2. The method as claimed in claim 1, further comprising

receiving the cache operation at a cache, wherein the cache operation requests data; and

returning a cache hit in response to the cache operation, wherein the cache has a pending fetch for the data in response to a prior cache operation requesting the data.

3. The method as claimed in claim 2, where in response to the prior cache operation, the data has been requested from memory but has not yet been stored in the cache at a time when the cache receives the cache operation.

4. The method as claimed in claim 3, wherein the cache operation includes a tag field maintained in a first phase of the two or more phases and a data field in a second phase of the two or more phases.

5. The method as claimed in claim 3, wherein the cache operation includes a tag field maintained in a first clock domain of the two or more clock domains and a data field in a second clock domain of the two or more clock domains.

6. The method as claimed in claim 3, further comprising returning the data from the cache once the data is available.

7. A device comprising:

a cache memory array; and

control logic coupled to the cache memory array, wherein the control logic divides a cache operation into two or more phases and two or more clock domains.

8. The device as claimed in claim 7, wherein the cache memory array:

receives the cache operation that requests data; and

returns a cache hit in response to the cache operation, wherein the cache array has a pending fetch for the data in response to a prior cache operation requesting the data.

9. The device as claimed in claim 8, wherein the control logic further comprises:

a decoder connected to the cache memory array; and

a controller connected to the decoder.

10. The device as claimed in claim 9, where in response to the prior cache operation, the data has been requested from memory but has not yet been stored in the cache at a time when the cache array receives the cache operation.

11. The device of claim 10, further comprising a DRAM controller integrated with the cache memory array.

12. The device of claim 11, further comprising an integrated graphics controller, a host AGP controller, and an I/O hub interface.

13. A computer-readable medium having stored thereon a plurality of instructions, said plurality of instructions when executed by a computer, cause said computer to perform the method of:

splitting a cache operation into two or more phases and two or more clock domains.

14. The computer-readable medium of claim 13, having stored thereon additional instructions, said additional instructions when executed by a computer, cause said computer to further perform the method of:

receiving the cache operation at a cache, wherein the cache operation requests data; and

returning a cache hit in response to the cache operation, wherein the cache has a pending fetch for the data in response to a prior cache operation requesting the data.

15. The computer-readable medium of claim 14, where in response to the prior cache operation, the data has been requested from memory but has not yet been stored in the cache at a time when the cache receives the cache operation.

16. The computer-readable medium of claim 15, wherein the cache operation includes a tag field maintained in a first phase of the two or more phases and a data field in a second phase of the two or more phases.

17. The computer-readable medium of claim 15, wherein the cache operation includes a tag field maintained in a first clock domain of the two or more clock domains and a data field in a second clock domain of the two or more clock domains.

18. The computer-readable medium of claim 15, having stored thereon additional instructions, said additional instructions when executed by a computer, cause said computer to further perform the method of returning the data from the cache once the data is available.

19. A system, comprising:

a system memory controller, comprising

a cache memory array, and

control logic coupled to the cache memory array, wherein the control logic divides a cache operation into two or more phases and two or more clock domains; and

system memory connected to the system memory controller.

20. The system as claimed in claim 19, further comprising

one or more interfaces connected to the system memory controller, including

an I/O hub interface connected to a bus,

a processor interface; and

a host AGP controller connected to the system memory controller via the bus;

wherein the cache array receives the cache operation requesting data via the one or more interfaces, and returns a cache hit in response to the cache operation, wherein the cache has a pending fetch for the data in response to a prior cache operation requesting the data.

21. The system as claimed in claim 20, where in response to the prior cache operation, the data has been requested from the system memory but has not yet been stored in the cache at a time when the cache receives the cache operation.

22. The system as claimed in claim 21, wherein the cache operation includes a tag field maintained in a first phase of the two or more phases and a data field in a second phase of the two or more phases.

23. The system as claimed in claim 21, wherein the cache operation includes a tag field maintained in a first clock domain of the two or more clock domains and a data field in a second clock domain of the two or more clock domains.